Intel Itanium Processor Technology and Roadmap Update

27th April 2011

OpenVMS 2011, Bad Homburg

Dr. Feixiong Liu
Senior Staff Engineer
Technical Account Manager for HP Servers
Intel EMEA
Feixiong.Liu@Intel.Com

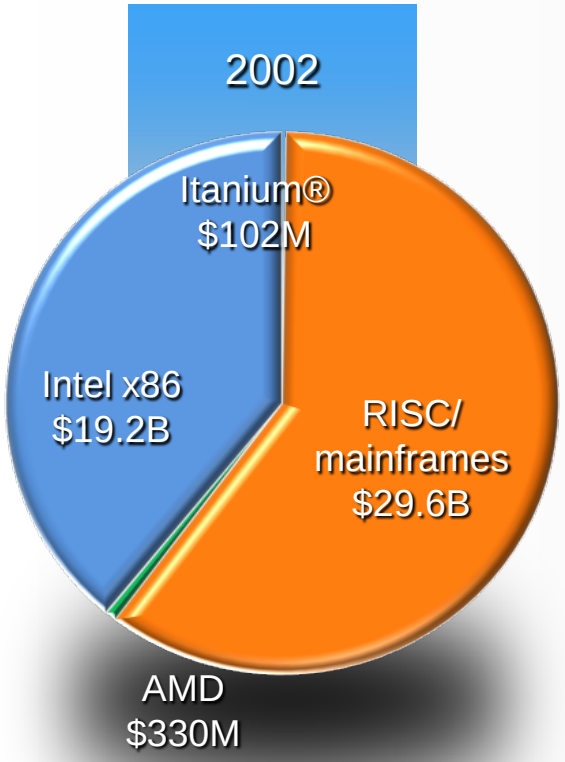
Legal Disclaimer

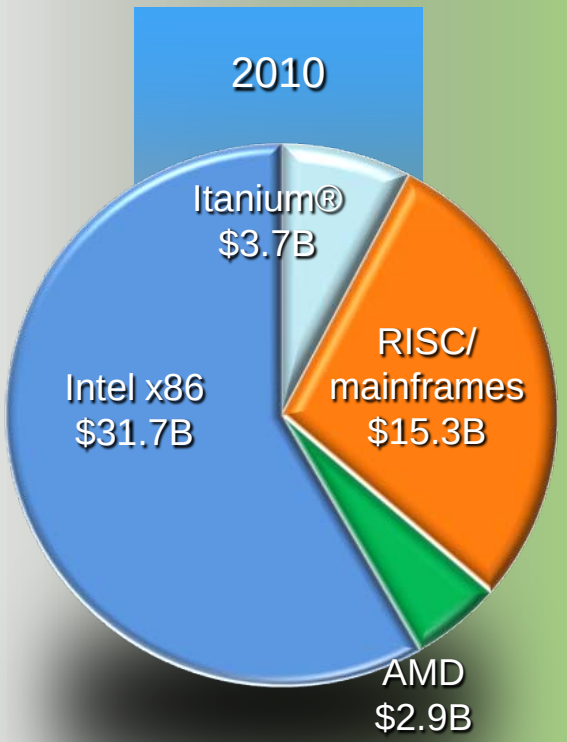
- INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL® PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. INTEL PRODUCTS ARE NOT INTENDED FOR USE IN MEDICAL, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS.
- Intel may make changes to specifications and product descriptions at any time, without notice.
- Intel does not control or audit the design or implementation of third party benchmarks or Web sites referenced in this document. Intel encourages all of its customers to visit the referenced Web sites or others where similar performance benchmarks are reported and confirm whether the referenced benchmarks are accurate and reflect performance of systems available for purchase.
- Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See www.intel.com/products/processor_number for details.
- Intel, processors, chipsets, and desktop boards may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available on request.
- Intel Virtualization Technology requires a computer system with a processor, chipset, BIOS, virtual machine monitor (VMM) and applications enabled for virtualization technology. Functionality, performance or other virtualization technology benefits will vary depending on hardware and software configurations. Virtualization technology-enabled BIOS and VMM applications are currently in development.
- Intel Turbo Boost Technology requires a system with Intel® Turbo Boost Technology capability. Consult your PC manufacturer. Performance varies depending on hardware, software and system configuration. For more information, visit http://www.intel.com/technology/turboboost
- 64-bit computing on Intel architecture requires a computer system with a processor, chipset, BIOS, operating system, device drivers and applications enabled for Intel® 64 architecture. Performance will vary depending on your hardware and software configurations. Consult with your system vendor for more information.
- Intel, Intel Xeon, Intel Core microarchitecture, and the Intel logo are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

Itanium® and the Mission Critical Biz Update

Source: IDC Q1'11 Worldwide Server Tracker (May'11)
(1) Source: HP 2010

Total: $49.3B
IA share: 39%



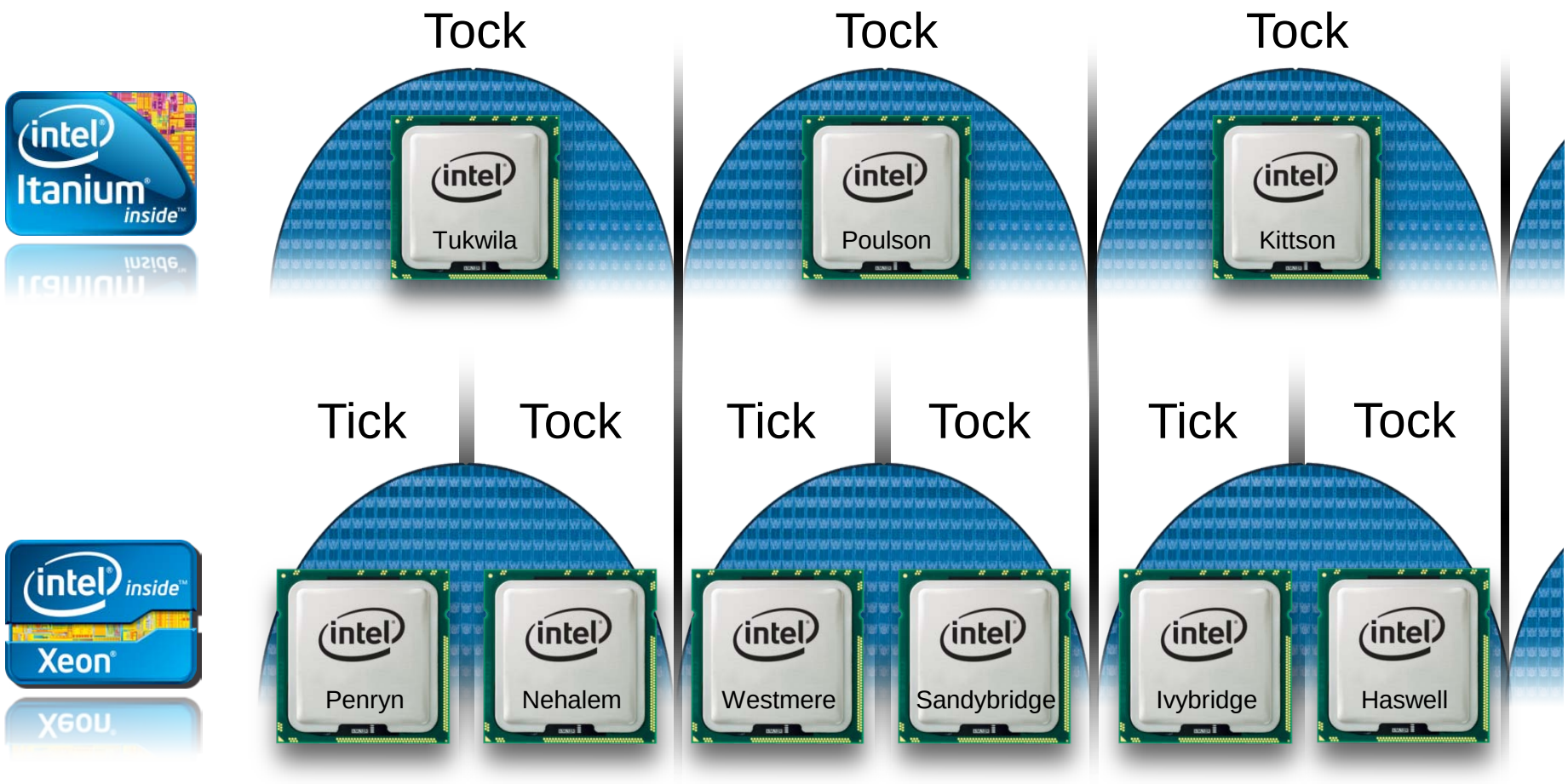


Total: $53.6B
IA share: 66%

More than 80% top Global 100 companies running Itanium (1)

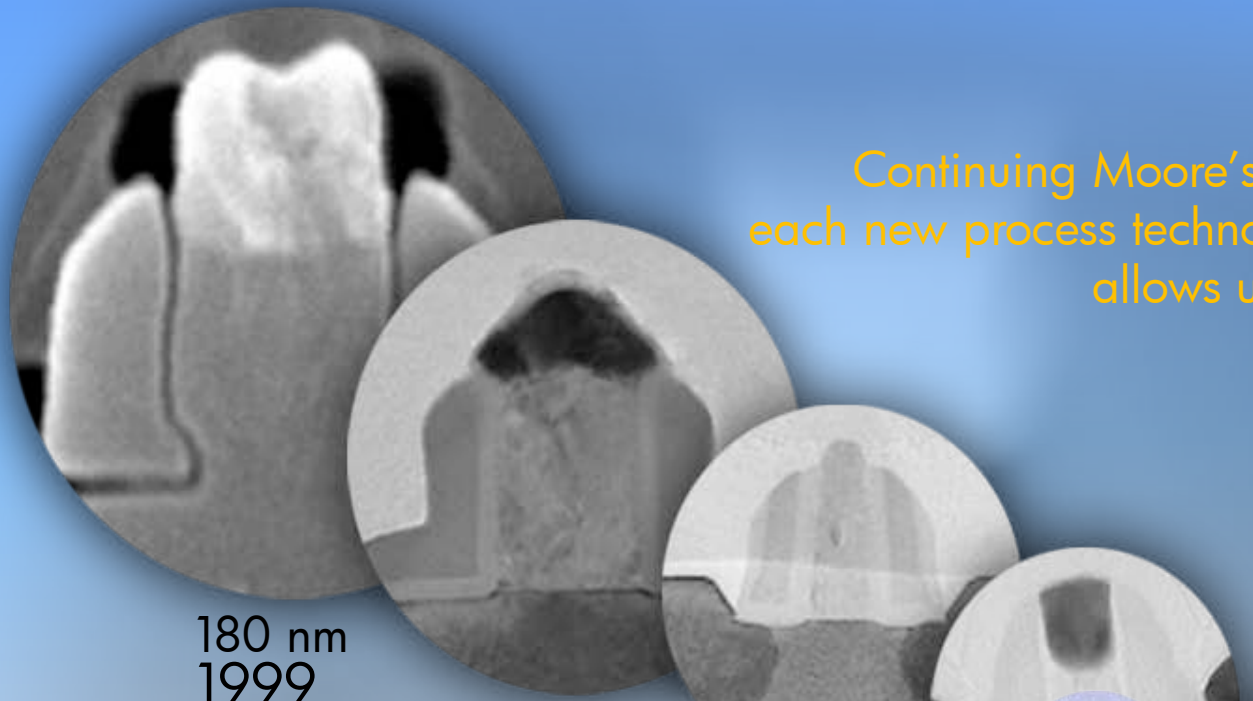
Predictable Tick-Tock Model

Sustained Server Microprocessor Leadership



All timeframes, products and dates are subject to change without further notification.

Moore's Law: Alive and Well at Intel



180 nm
1999

130 nm
2001

90 nm
2003

65 nm
2005

45 nm
2007

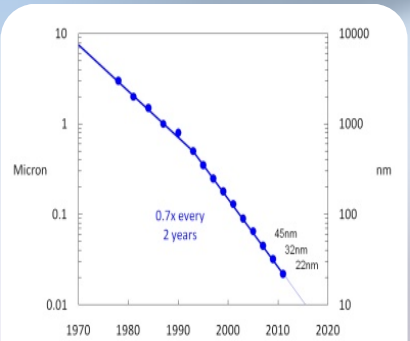
32 nm
2009

22 nm
2011

Continuing Moore's Law each new process technology allows up to:

Transistor Performance
+20%

Switching Power
-30%



Caption: Transistor dimensions scale to improve performance, reduce power and reduce cost per transistor.

Production

Development

Research

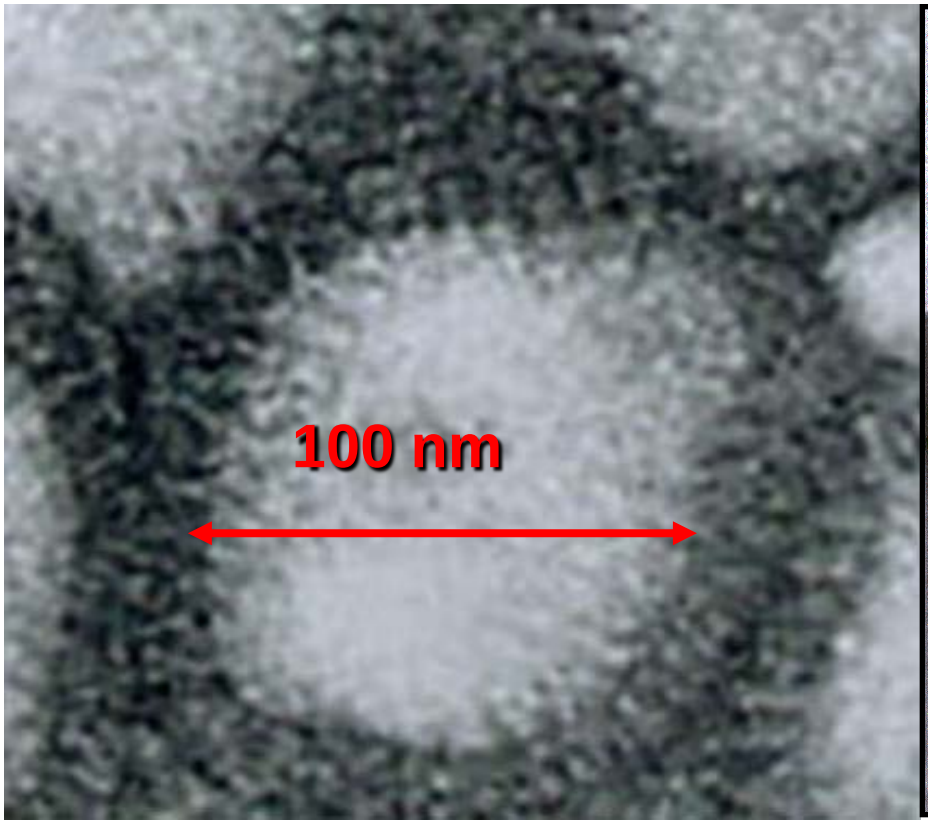
On Track

15nm

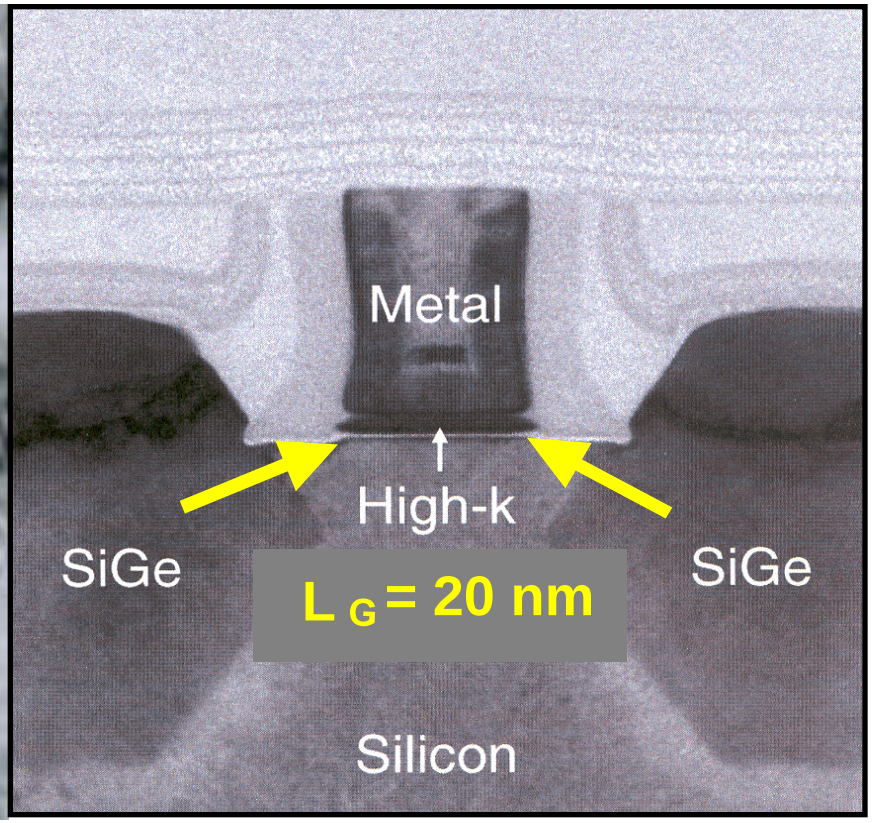
Potential
actual

All Intel products benefit from Intel's deep investment in advanced silicon manufacturing technologies

2.3 Billion Transistors on the Intel Xeon 7500 CPU
Each Transistor is 5x smaller than an Influenza Virus



100nm Influenza virus
Source: CDC



20 nm gate length (L_G=20) Intel Transistor

They all have to work!

Complete Line of Mission Critical Offerings connected by the Common Platform Strategy

Flexibility and Choice for a new Era in Mission Critical Computing

Family of Mission Critical Processors

Choice of Architecture Based on:

Hardened Operating System	✓
Application Availability	✓
OEM System Capability	✓
OEM Service & Support	✓

Itanium 9300 Series

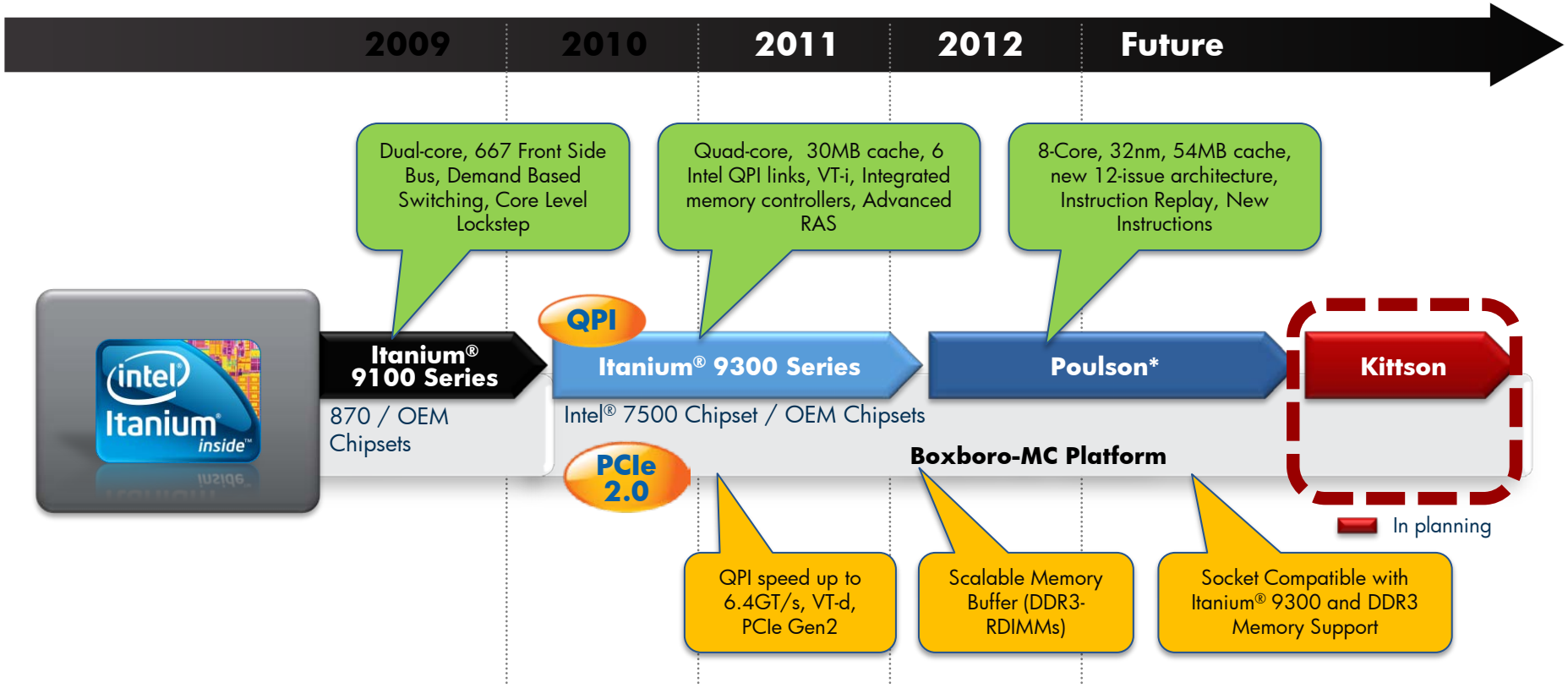
Architected for Mission Critical UNIX with mainframe resiliency and scalability

Xeon E7 Series

Architected for scalable Windows and Linux performance with advanced reliability

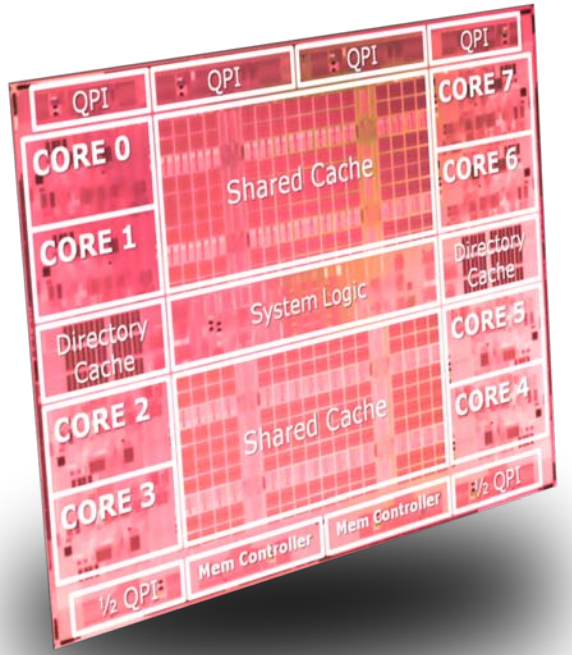
Two Server Platforms to meet a wide range of Mission Critical Requirements

Intel® Itanium® Platform Roadmap



- Poulson program on track and silicon is going through early post-silicon characterization
- Product availability is targeted for 2012

Poulson: Advances Itanium® Architecture



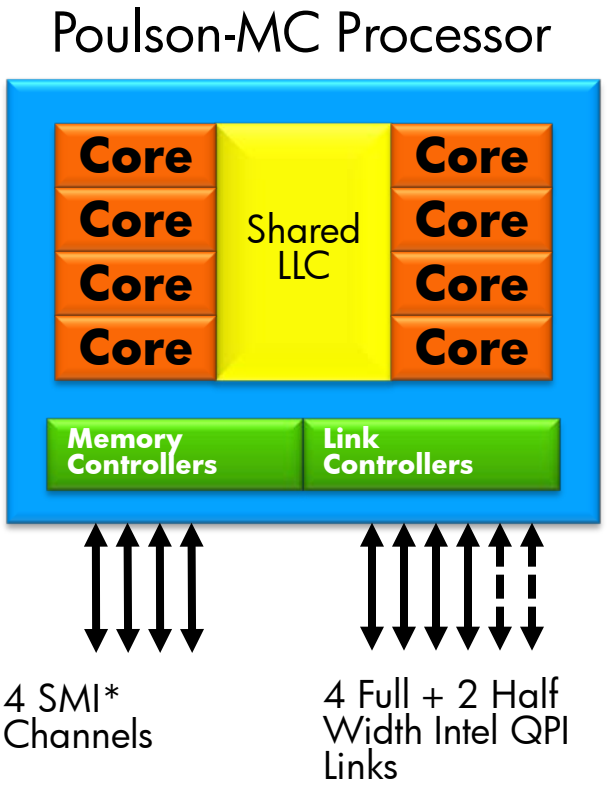
Key Highlights

- New Micro-architecture, 2x the cores, 2x instructions throughput
- Socket and Binary Compatible with Itanium® 9300 processors (Tukwila)
- 3.1 Billion Transistors on 32nm process
- Total 54MB on-die memory
- Intel® Instruction Replay Technology
- Intel® Hyper-Threading Technology, enhanced with dual-domain multi-threading support
- Intel® Itanium New Instructions

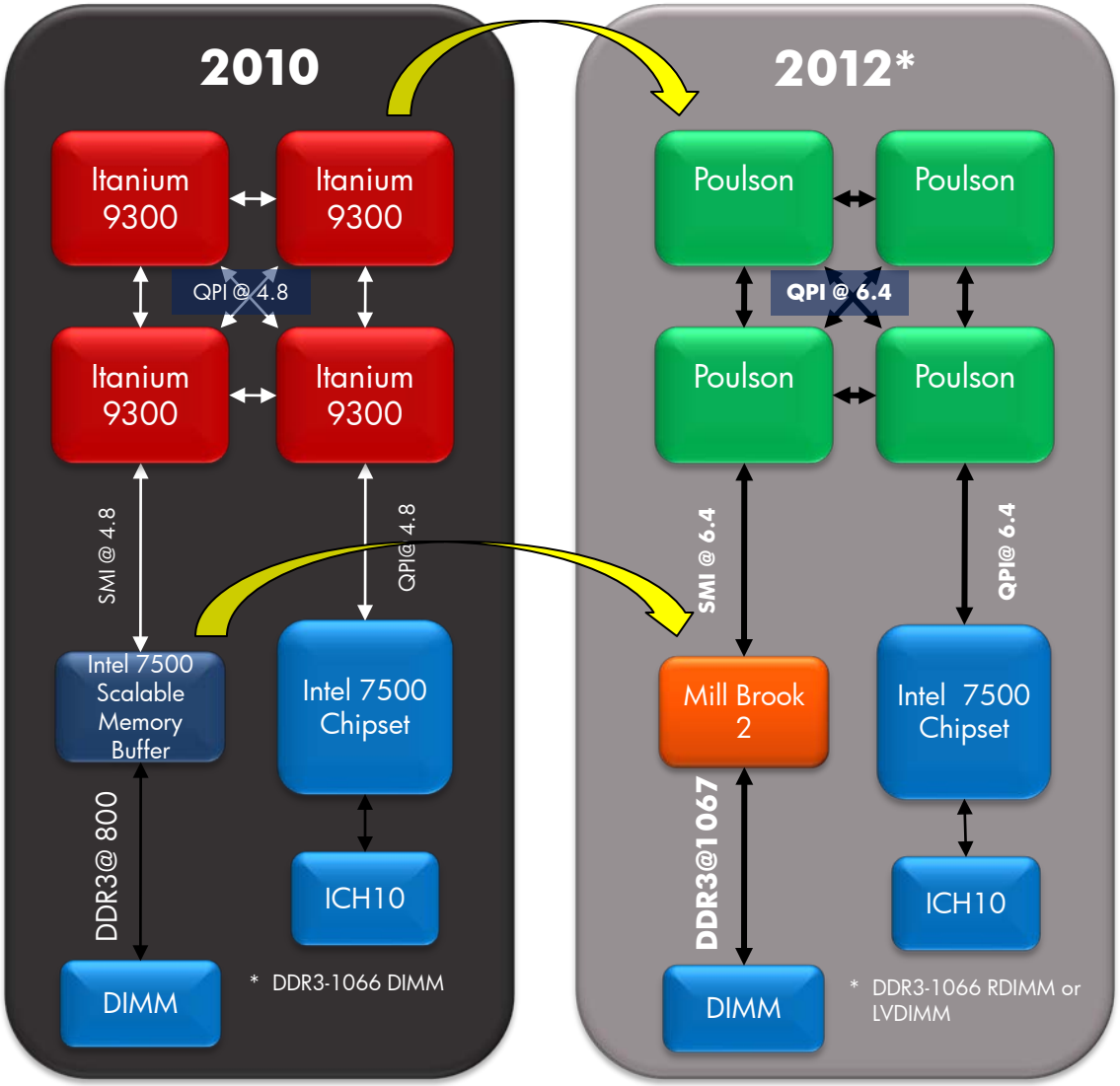
Poulson: the most sophisticated Intel® processor to date

The Poulson-MC Processor Architecture Overview

- Up to 8 cores per socket
- Up to 32 MB **shared** Last Level Cache (LLC)
- 2 integrated memory controllers supporting Intel® SMI* running at 6.4 GT/s
  - 45 GB/s Memeory Bandwidth/Socket
- 4-full and 2-half width Intel QuickPath® Interconnects running at 6.4 GT/s
  - 128 GB/s Communication Bandwidth/Socket
- 2 Directory caches
- Supports enhanced Hyper-threading
- Supports new RAS features
- Power/thermal variants targeting:
  - 170W, 155W, 130W



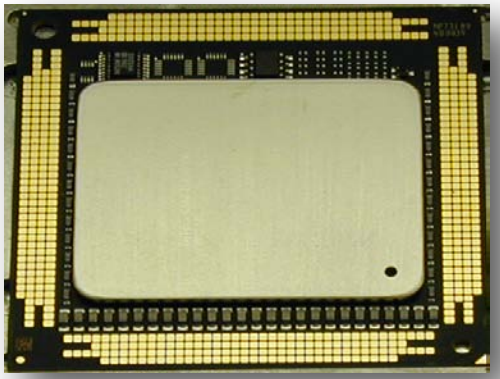
Poulson Platform vs. Tukwila Platfrom



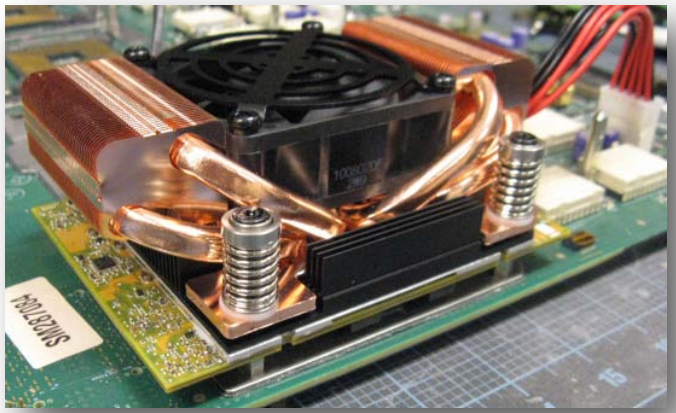
- New Micro-Architecture CPU (Poulson)
- New Scalable memeory buffer (Mill Brook2)
  - Low Voltage DIMM and 1066 MHz support
- Faster QPI speed(CPU-CPU, CPU-IOH)
  - 6.4 GT/s vs. 4.8 GT/s
- Faster SMI speed
  - 6.4 GT/s vs. 4.8 GT/s

*Platform availability

Poulson Processors

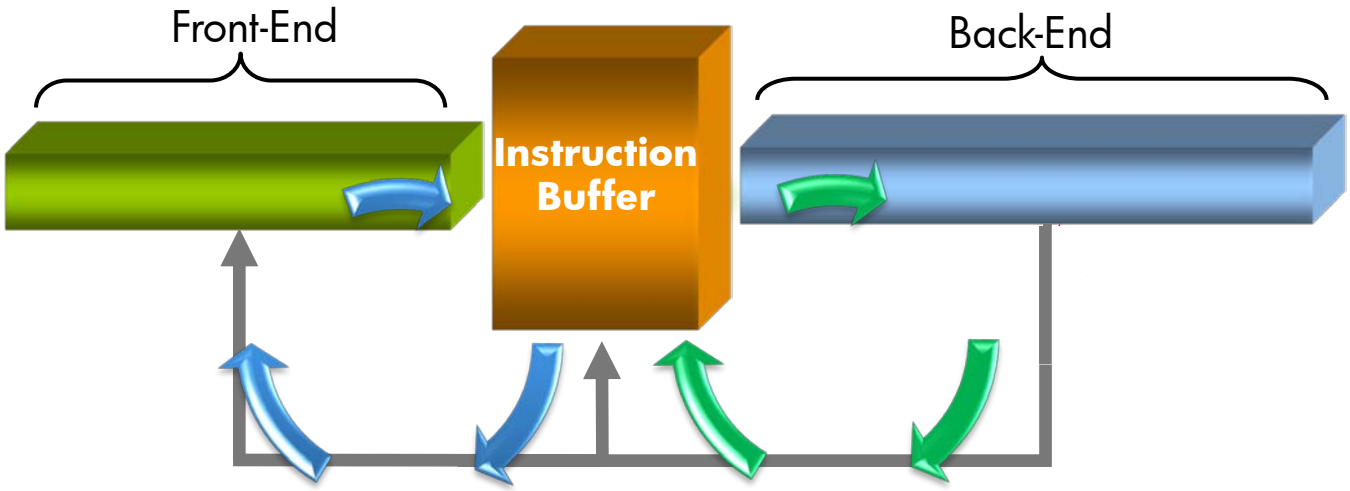


Poulson Package



Poulson in a system

Next Generation Micro-Architecture



Key New Features

- **Instruction Replay** automatically recovers from severe errors to improve resiliency
- **Enhanced Hyperthreading** enables concurrent operations on different threads and improves performance

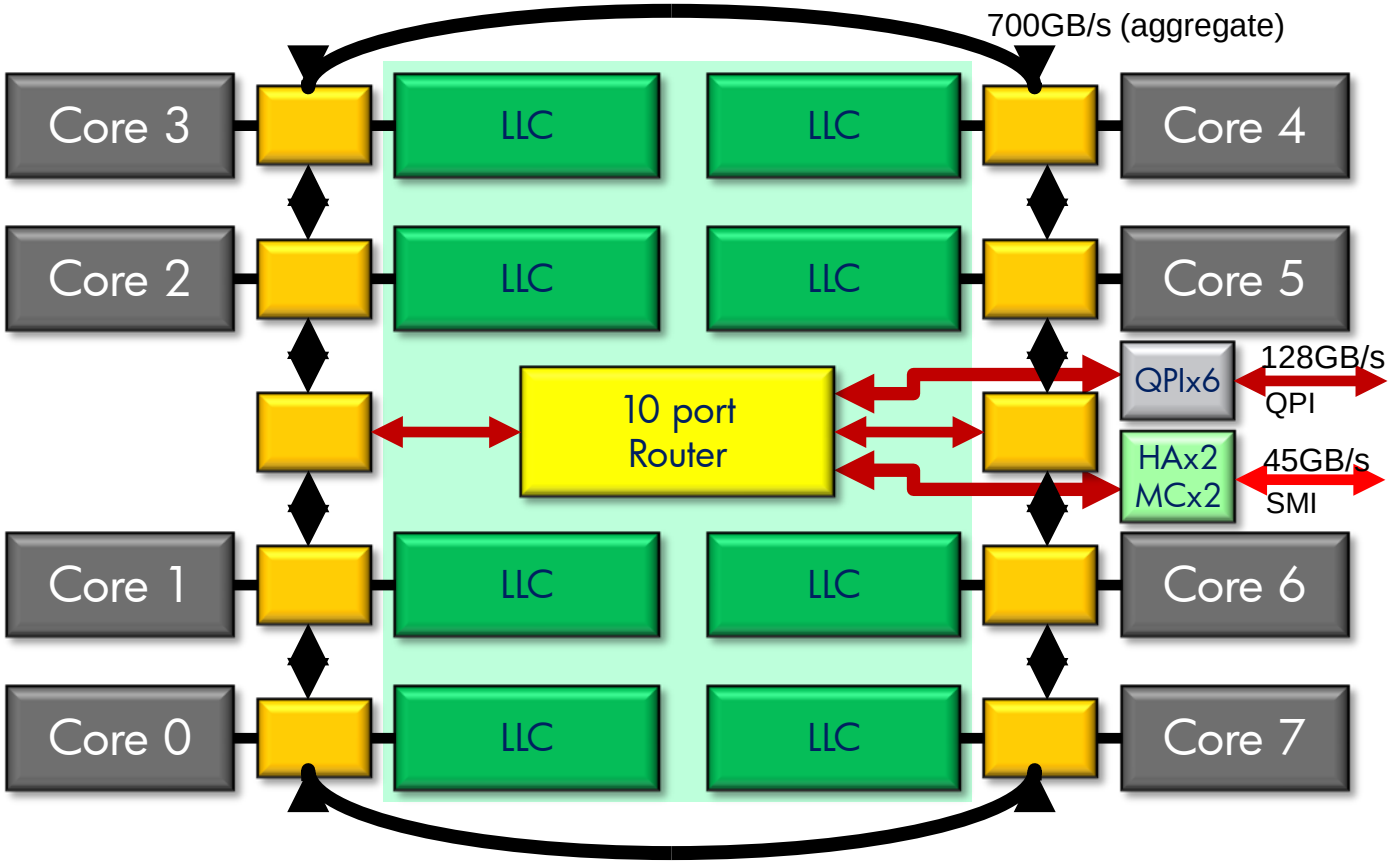
ew architecture brings a leap in performance and process resilien

Exploiting Parallelism on All Levels

- Multi-core Parallelism/Multi-socket Parallelism
- Thread Parallelism
- Instruction Level Parallelism
- Memory Parallelism

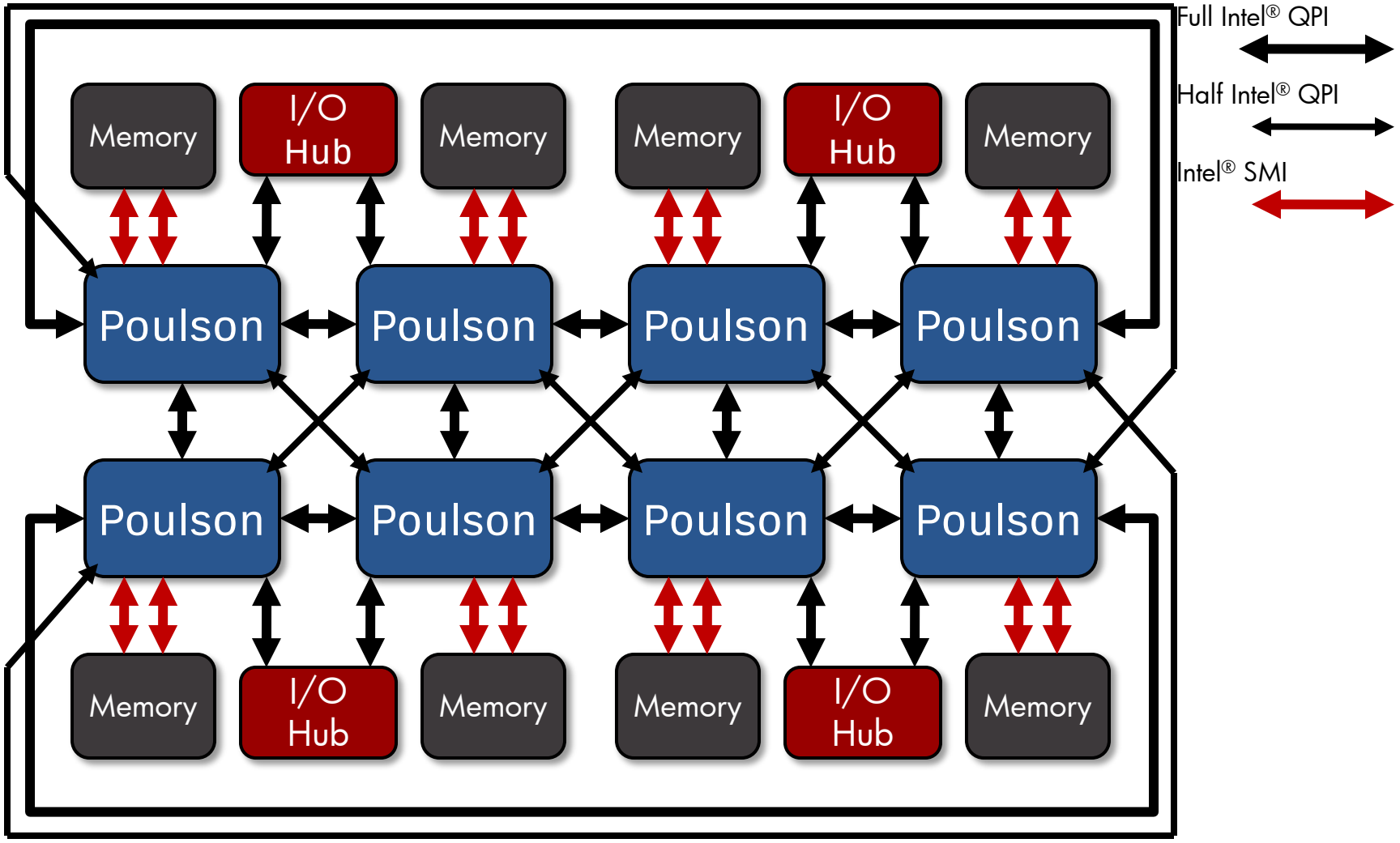
Multi-level parallelism exposed to software control

Multi-core and Multi-socket Parallelism



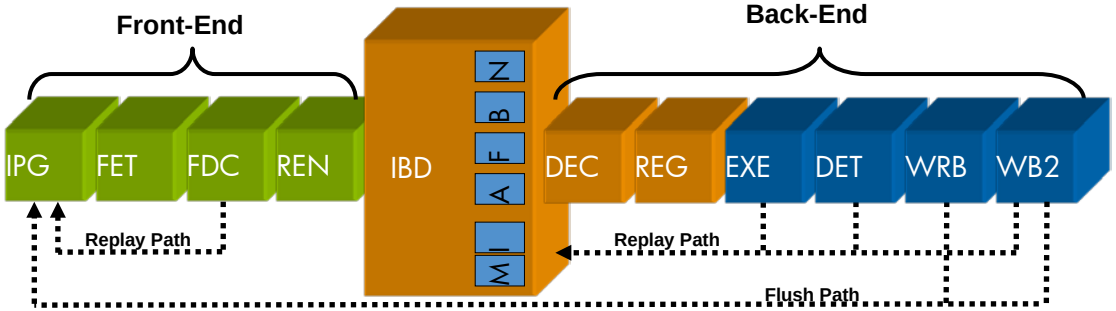
New bi-directional high-bandwidth ring interconnect

Example 8-Socket Topology



Hyper-Threading Technology Improvements

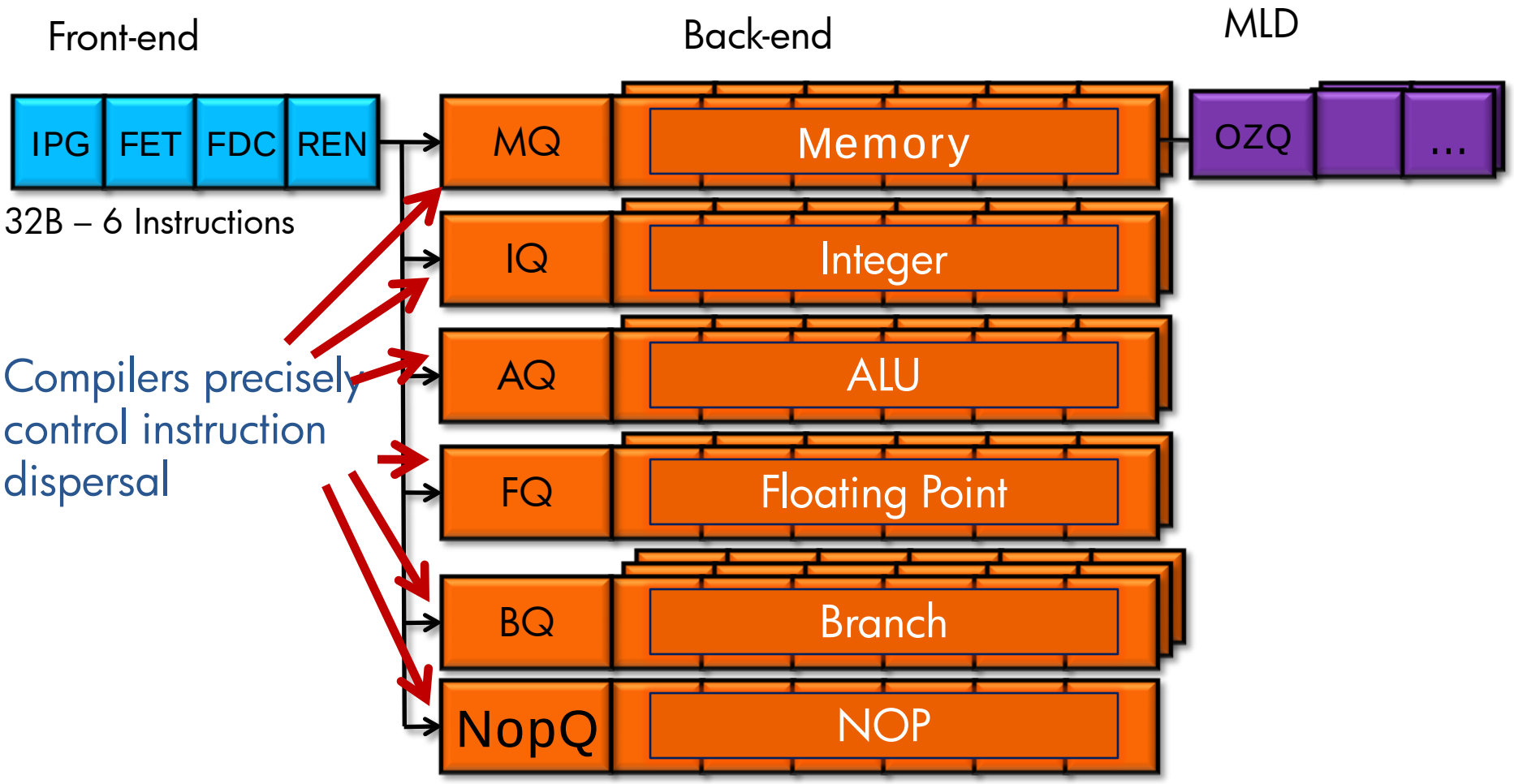
- Dual-domain multi-threading combines elements of SOEMT (Switch-on-event) and SMT (Simultaneous) multi-threading



- Front-end and back-end can operate on different threads
- IBD stores 96 instructions per thread (96x2 queue entries)
  - Maximizes efficiency of concurrent threads to drive 12-wide issue
- Front-end and back-end can switch threads on different conditions

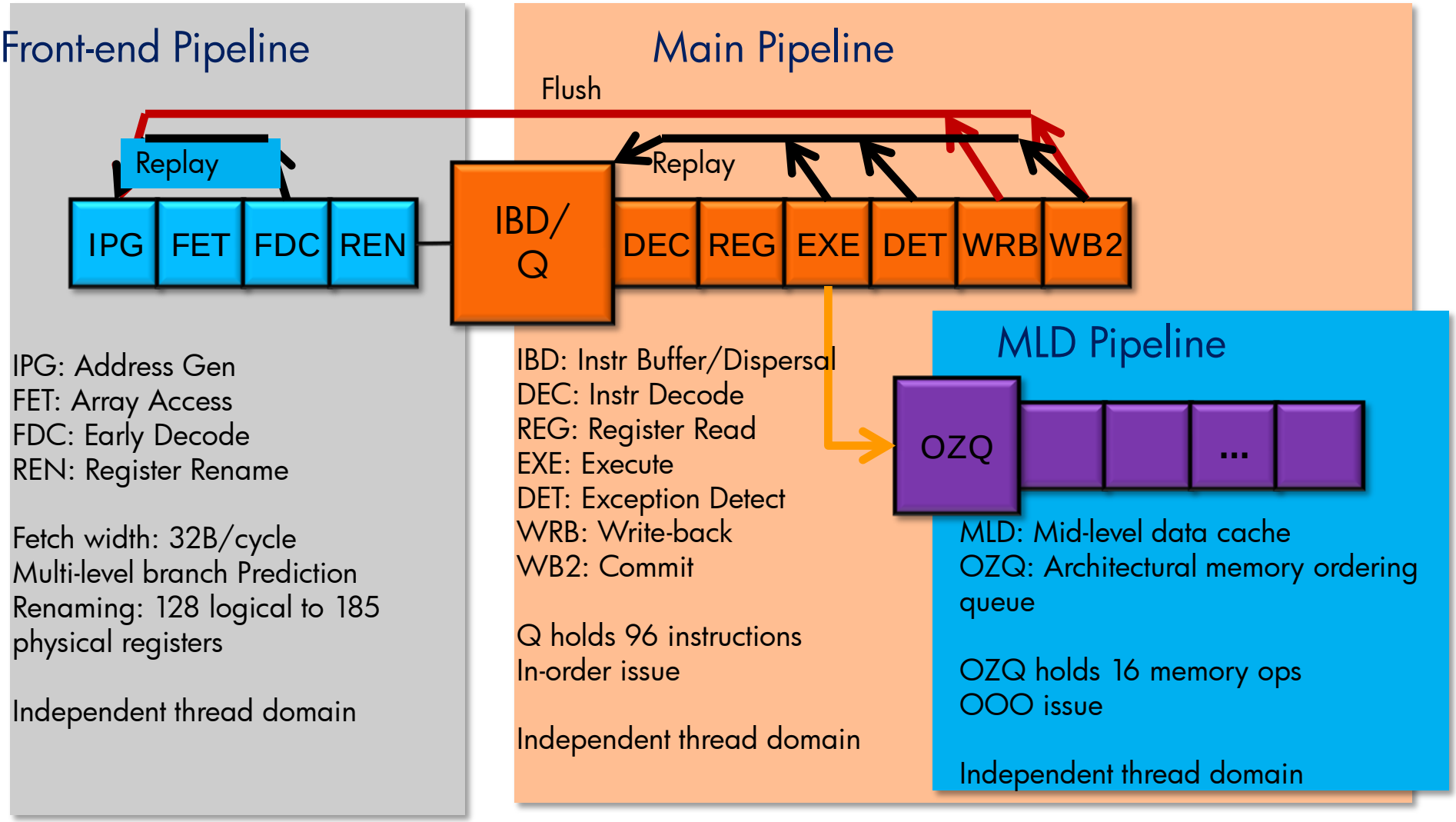
Dual-Domain Multi-Threading support enhances MT performance

Instruction Parallelism



12-wide issue under software control

Instruction Parallelism and memory parallelism



Concurrency via 3 decoupled pipelines

Memory Parallelism – Avoiding Hazards

–Expanded Software Hints
- Provides control over allocation, speculation and prefetch policies
- Multi-line software prefetch

–Reduced Speculation Costs
- Spontaneous Deferrals on speculative loads
- Deferred load can transform into a prefetch to cache and/or TLB

–New Hardware Prefetcher
- Into FLD and/or MLD
- Adaptive based on FLD/MLD miss patterns

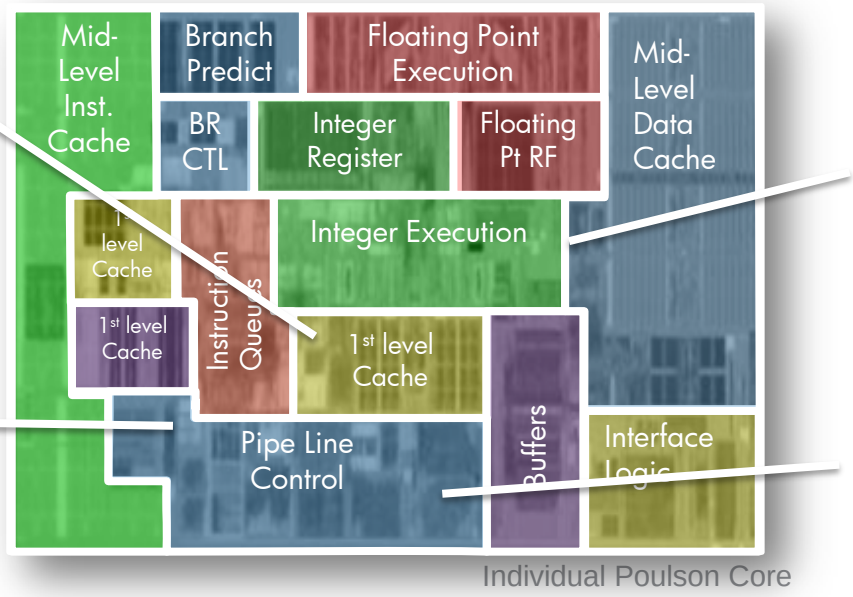
–Reduced Data Hazards
- Expanded store to consumer bypassing in FLD and MLD
- Single-cycle MLD to FLD line transfers

Pipeline bottlenecks removed

Itanium® Processor New Instructions

Expanded Data Access Hints
- mov dahr

Thread Control
- hint@priority



Individual Poulson Core

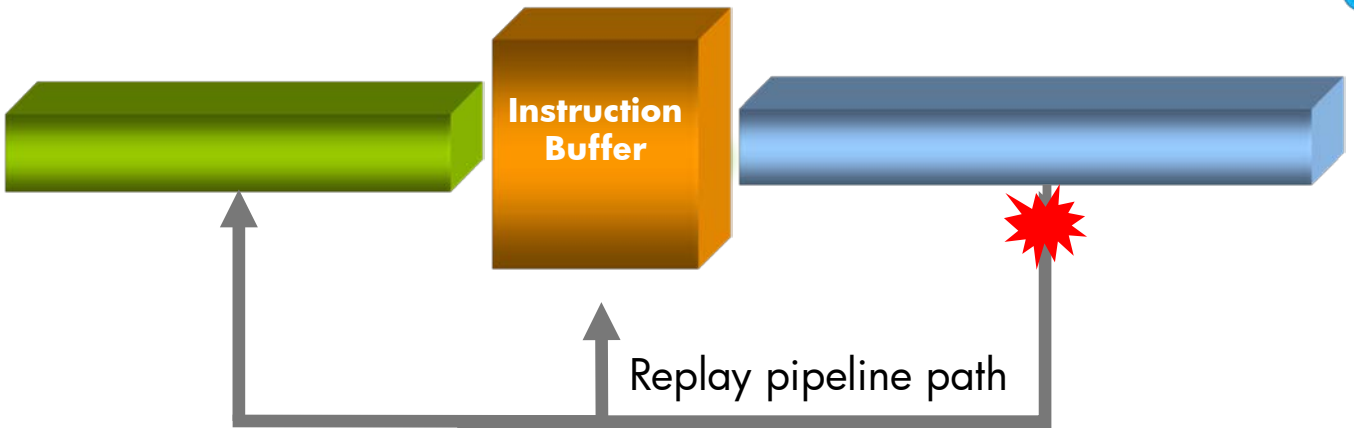
Integer Operations
- mpy4
- mpyshl4
- clz

Expanded Software Prefetch
- ifetch.count

- Poulson continues to optimize for legacy Itanium code without recompilation
- Recompilation can yield some additional performance upside

New Instructions enable performance improvements

Key RAS feature: Instruction Replay



- Front-end data integrity errors (e.g., rename parity error) resolved with front-end replay path and instruction re-fetch
- Back-end data integrity errors (e.g., FP residual error) resolved by reissuing instruction from IBD
- IBD parity error resolved by flush of full pipeline and instruction re-fetch

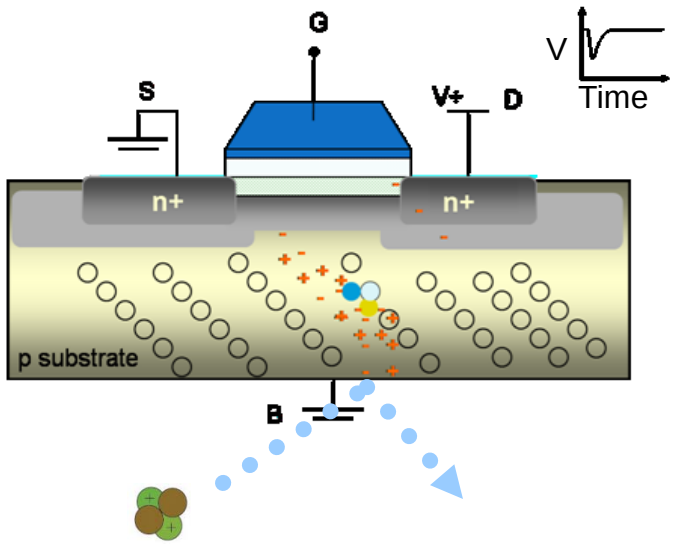
Instruction Replay Technology avoids system crashes and data corruption to increase service reliability

Reliability, Fault Tolerance and Recoverability

- Intel® Instruction Replay Technology
  - Main pipeline redesigned for error handling
  - Enabled hardware and firmware recovery of correctable errors
- Increased Error Detection and Correction
  - Arrays
    - MLI, MLD, LLC tag and Directory cache – SECDED
    - LLC data – DECTED
    - Register files (GR and FR) – SECDED
  - Logic path error detection in FP ALU via residues
  - Key paths are protected “end to end” with invalidation and replay
- Reworked Error Detection, Response and Reporting Framework
  - Large increase in error detection and response capabilities
  - Increased hardware responses and recovery
  - Intel® Cache Safe Technology: lockout of failing cache locations

Special Circuit Topology Reduces and prevents Soft Errors

Outside of human errors, Soft Errors are one of the most common causes of server errors. Intel Itanium processors are designed to reduce and prevent Soft Errors.



Device under a random particle strike, causing a soft error

Mission Critical Solutions require special designs in hardware and software to prevent, contain, and recover from soft errors

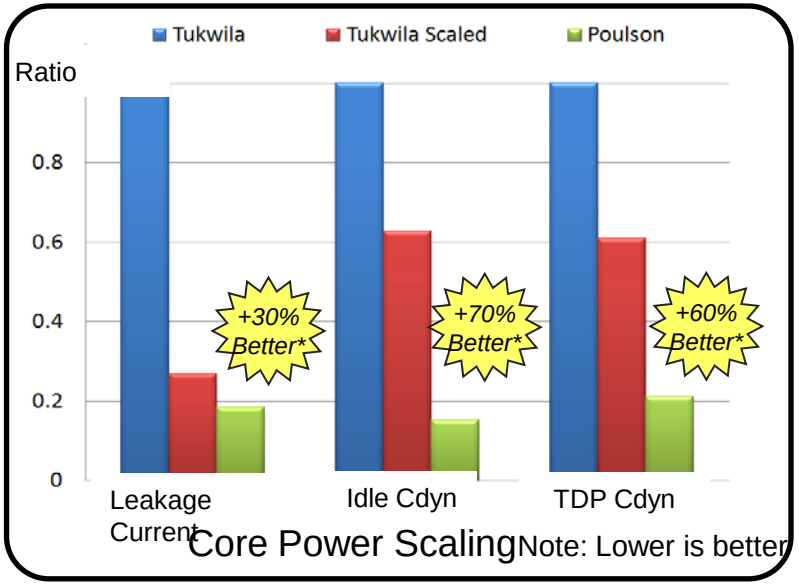
Poulson RAS Improvement Summary

	Itanium 9300	Poulson
LLC Data	SECDEC	DECTED
LLC Tags	SECDEC	SECDED
MLI Data & Tags	Parity w/inval	SECDED
MLD Data & Tags	SECDED	SECDED
Directory Cache	Parity w/inval	SECDED
Integer/Floating Point Registers	Parity	SECDED
IBD	None	Parity w/replay
FPU Adders and Multipliers	None	Residual
End-to-End Data Detection	No	Yes
Memory Controller	x4=DDDC, x8=SDDC	x4=DDDC, x8=SDDC
Memory Sparing	DIMM	Rank
SMI lane/clock failover	Reduced ECC	Full ECC

Poulson has further enhanced the already strong Itanium® RAS capability

Power Enhancements

- Techniques
  - Removal of dynamic logic
  - Stall -> Replay architecture
  - Aggressive clock gating



Power reductions and active power management improve scaling well beyond traditional technology scaling

Early Thoughts on Next-Generation Itanium (Kittson)

- Team is ramping up on definitional work
- Core will leverage Poulson core pipeline redesign investment
  - Leverage process advancements
  - Binary compatibility with Itanium ISA
- Targeting significant throughput improvement & thread-level improvement
- Platform definition in progress
  - Continue to follow common platform vision
  - Continue to share components with Xeon
  - Continue to provide OS and vender flexibility to Mission Critical customers

Kittson Development continues Intel's On-Going Commitment to Itanium Product Line

Summary

- Poulson new architecture for mission critical workloads
- Intel and HP are committed to future of Itanium computing. Itanium product line is on a standard planning cycle
- Intel and HP are working closely in silicon characterization and system validation
- Poulson processor is on track for product availability in 2012